

	L #	Hits	Search Text	DBs	Time Stamp
1	L1	1836	(438/270).CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 08:59
2	L2	1794	1 and ((@ad<"20030801") or (@rlad<"20030801"))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:13
3	L3	42	2 and collar	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:13

	L #	Hits	Search Text	DBs	Time Stamp
4	L4	1360	capacitor near8 ((lower or bottom) near4 trench)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:14
5	L5	38	2 and 4	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:14
6	L7	15	5 not 3	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:18

	L #	Hits	Search Text	DBs	Time Stamp
7	L8	58886	(international adj business adj machines adj corporation)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:22
8	L9	182	8 and 4	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:22
9	L10	139	9 and collar	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:22

	L #	Hits	Search Text	DBs	Time Stamp
10	L11	131	10 and ((@ad<"20030801") or (@rlad<"20030801"))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:44
11	L12	639	(438/386).CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:50
12	L13	181	12 and 4	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:50

	L #	Hits	Search Text	DBs	Time Stamp
13	L14	6599	(bottle-shaped) or (bottle near shaped) or (bottle near shape)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:51
14	L15	44	13 and 14	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:51
15	L16	36	15 not 11	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:51

	L #	Hits	Search Text	DBs	Time Stamp
16	L17	30	16 and ((@ad<"20030801") or (@rlad<"20030801"))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 09:58
17	L18	278	(438/387).CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:01
18	L19	53	18 and 4	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:01

	L #	Hits	Search Text	DBs	Time Stamp
19	L20	48	19 and ((@ad<"20030801") or (@rlad<"20030801"))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:01
20	L21	48	20 not 3	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:01
21	L22	44	21 not 16	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:02

	L #	Hits	Search Text	DBs	Time Stamp
22	L23	44	22 not 17	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:08
23	L25	1812	Akatsu.in.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:09
24	L26	5	25 and 4	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:10

	L #	Hits	Search Text	DBs	Time Stamp
25	L27	26432	Cheng.in.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:10
26	L28	32	27 and 4	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:10
27	L29	20	28 and collar	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:11

	L #	Hits	Search Text	DBs	Time Stamp
31	L33	238	32 and 4	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:13
32	L34	201	33 and ((@ad<"20030801") or (@rlad<"20030801"))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:13
33	L35	6	34 and overhang	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:14

	L #	Hits	Search Text	DBs	Time Stamp
34	L37	190	34 and nitride	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:14
35	L38	278	(438/387) .CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 10:15

	L #	Hits	Search Text	DBs	Time Stamp
1	L1	739	(438/243).CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 18:13
2	L2	206	((widened or wider or larger or bigger) near4 trench) and collar and (DRAM or "dynamic random access memory" or memory)	US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B	2005/06/23 18:26

US-PAT-NO: 6716696

DOCUMENT-IDENTIFIER: US 6716696 B2

TITLE: Method of forming a bottle-shaped trench in a semiconductor substrate

----- KWIC -----

Application Filing Date - AD (1):
20020726

Brief Summary Text - BSTX (6):

However, as the size of a DRAM is scaled down by a factor of f (feature size), the trench storage node capacitance decreases by a factor of f . Therefore, it is important to develop methods to increase the storage capacitance. One method employed to increase capacitance is to widen the bottom portion of the trench, thus, increasing the surface area and creating a "bottle shaped" capacitor. However, in order to space the capacitors close together, control of the etching process used to widen the bottom portion becomes a governing factor. Chemical dry etching is predominantly used in the prior art for creating the bottle-shaped portion of the capacitor. In U.S. Pat. No. 5,112,771 issued to Ishii, et al. on May 12, 1992, entitled, "METHOD OF FABRICATING A SEMICONDUCTOR DEVICE HAVING A TRENCH", the bottom region of a trench capacitor is enlarged. This is accomplished by leaving a silicon oxide film on the upper sidewall of a trench, and enlarging the width of the exposed bottom portion of the trench by an isotropic dry etching process. Since the silicon substrate is isotropically dry etched, it is etched not only in the vertical direction to the surface of the substrate, but also in the horizontal direction. Although the capacitor surface area is enlarged, the etching processes are not easily controlled.

US-PAT-NO: 6448131

DOCUMENT-IDENTIFIER: US 6448131 B1

TITLE: Method for increasing the capacitance of a
trench
capacitor

----- KWIC -----

Application Filing Date - AD (1):
20010814

Assignee Name - ASNM (1):
International Business Machines Corporation

Assignee Group - ASGP (1):
International Business Machines Corporation Armonk NY 02

Brief Summary Text - BSTX (19):
These and other objects and advantages are achieved in the present invention by utilizing a method wherein the increased trench capacitor surface area is obtained by roughening the interior walls (sidewalls and bottom trench wall) of the trench using a metal silicide as a roughening agent.

Brief Summary Text - BSTX (20):
Specifically, the method of the present invention comprises the steps of:
(a) forming a trench in a Si-containing substrate, said trench having an upper region, a lower region and interior walls including sidewalls which extend to a common bottom wall; (b) forming a collar region in said upper region of said trench; (c) forming a metal layer (lumpy or continuous and uniform) on at least a portion of exposed interior walls of said trench; (d) annealing said metal layer so as to form a metal silicide layer; and (e) removing said metal silicide layer so as to provide roughened trench walls.

Detailed Description Text - DETX (11):
At this point of the present invention, and as shown in FIG. 1C, collar

region 24 may be formed in upper region 16 of one or more trench openings 14.

Collar region 24 may also be omitted in some embodiments of the present invention. When collar region 24 is present, it is formed utilizing conventional processing techniques well known in the art. For example, the collar region may be formed by deposition or thermally growing a collar material such as tetraethylorthosilicate (TEOS). In one embodiment of the present invention, the collar region may include an oxide collar having a nitride layer formed thereon.

Detailed Description Text - DETX (12):

Following the formation of the collar region, lower region 18 of trench opening 14 may be optionally subjected to an isotropic etching process which is capable of forming a trench which contains a broadened lower region that laterally extends outward from sidewalls 20. This embodiment of the present invention is not shown in the drawings, but is nevertheless contemplated herein.

Detailed Description Text - DETX (14):

Next, and as illustrated in FIG. 1D, metal layer 26 is formed at least in lower region 18 of trench opening 14 on the interior trench walls including sidewalls 20 and bottom wall portion 22. Note that in the drawings, the metal layer is formed in the upper region on collar region 24 as well as hardmask 12. The metal layer formed at this point of the present invention may be a continuous and uniform layer, or the metal layer is comprised of islands, i.e., granules or lumps, that may or may not be in contact with neighboring islands.

Detailed Description Text - DETX (23):

Following the annealing step, any unreacted metal (including metal on the Si-containing substrate as well as hardmask and collar) is removed utilizing a conventional selective etching process that is well known in the art.

Note

that in some embodiments of the present invention the possibility exists that during the annealing step all of the metal is consumed within the trenches.

This is typically the case on a production line since the annealing conditions

are selected so as to consume all the metal formed on the interior walls of the

trenches. In embodiments wherein the metal is not completely consumed inside

the trenches, any wet etch process may be used in removing unreacted metal from

the trench. The chemical etchant employed in the wet etch process is highly

selective in removing unreacted metal as compared with either hardmask

material, collar material, Si and silicide material. A suitable etchant that

can be employed at this point of the present invention is a mixture of hydrogen

peroxide and nitric or sulfuric acid. Other chemical etchants are also

contemplated herein. Note that the wet etch process mentioned above also

removes metal from atop the hardmask as well as the collar region.

Claims Text - CLTX (4):

4. The method of claim 5 wherein said collar region is formed by deposition of at least one dielectric material.

Claims Text - CLTX (5):

5. The method of claim 1 further comprising forming a collar region in said upper region of said trench prior to forming said metal layer.

Claims Text - CLTX (26):

26. A method of increasing the surface area of a trench, without widening the dimension of the trench, said method comprising the steps of: (a) forming a trench in a Si-containing substrate, said trench having an upper region, a lower region and interior walls including sidewalls which extend to a common bottom wall; (b) forming a collar region in said upper region of said trench; (c) forming a metal layer on at least a portion of exposed interior walls of

said trench; (d) forming a Si-containing layer on said metal layer; (e) annealing said metal layer so as to form a metal silicide layer; and (f) removing said metal silicide layer so as to provide roughened trench walls.

Claims Text - CLTX (28):

28. A method of increasing the surface area of a trench, without widening the dimension of the trench, said method comprising the steps of: (a) forming a trench in a Si-containing substrate, said trench having an upper region, a lower region and interior walls including sidewalls which extend to a common bottom wall; (b) forming a collar region in said upper region of said trench; (c) forming a metal layer on at least a portion of exposed interior walls of said trench; (d) annealing said metal layer so as to form a metal silicide layer; (e) forming a Si-containing layer on said metal layer and annealing said Si-containing layer so as to diffuse said Si-containing layer through said metal silicide layer; and (f) removing said metal silicide layer so as to provide roughened trench walls.

Claims Text - CLTX (32):

32. A method of increasing the surface area of a trench said method comprising the steps of: (a) forming a trench in a Si-containing substrate, said trench having an upper region, a lower region and interior walls including sidewalls which extend to a common bottom wall; (b) forming a collar region in said upper region of said trench; (c) forming SiGe islands in at least said lower region of said trench, (d) forming a metal layer on at least a portion of exposed interior walls of said trench not containing said SiGe islands; (e) annealing said metal layer so as to form a metal silicide layer; and (f) removing said metal silicide layer and said SiGe islands so as to provide roughened trench walls.